

Notice of Allowability

Application No.

10/619,601

Examiner

Ernest F. Karlsen

Applicant(s)

MIZUNO ET AL.

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the filing of July 16, 2003.
2. ☒ The allowed claim(s) is/are 1-14.
3. ☒ The drawings filed on 16 July 2003 are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 09/390,962.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date 0703, 0903
4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.


ERNEST KARLSEN
PRIMARY EXAMINER

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Claim 1, line 4, "MOD" has been changed to -- MOS -- to correct a typographical error.

In the specification, line 2, before "which". -- now U.S. Patent No. 6,630,857, -- has been inserted.

Reasons for Allowance

No reference was found anticipating or a combination of references found making obvious a test method of a semiconductor integrated circuit device comprising providing a semiconductor IC device having a logic circuit with a normal operation supply voltage, applying substrate bias voltages to MOS transistors of the logic circuit to increase threshold voltages of the MOS transistors and measuring the power supply current while the MOS transistors of the logic circuit are in a stationary state and while a voltage lower than the normal operation supply voltage is applied as the supply voltage. No reference was found anticipating or a combination of references found making obvious a test method of a semiconductor integrated circuit device comprising providing a semiconductor IC device including a logic circuit wherein for normal operation the supply voltage of the logic circuit is a first voltage and for normal operation an absolute value of a threshold voltage of a MOS transistor of the logic circuit is a second voltage

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and executing an IDDQ test of the semiconductor IC device while the supply voltage is set to be a third voltage lower than the first voltage and the absolute value of the threshold voltage is set to a fourth voltage higher than the second voltage.

Examiner's Comment

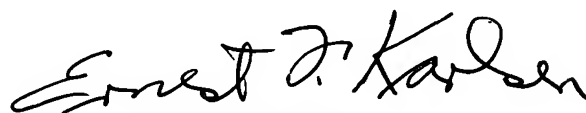
Claims 1-14 are allowed.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jennion et al and Palusa are cited to show prior art testing of integrated circuit devices wherein plural power supply voltages are applied during the test process.

Any inquiry concerning this communication should be directed to Ernest F. Karlsen at telephone number 571-272-1961.

Ernest F. Karlsen

September 17, 2004


ERNEST KARLSEN
PRIMARY EXAMINER